CB\_CTRL

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision Number | Date | Description of Change | Author |
| V0.0 | 9/23/2022 | Draft version | Shaoqiang |
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# CB\_CTRL

## Introduction

Balancing the cells maximizes the capacity of the battery pack and ensures that all energy is available, increasing the life of the battery. CB\_CTRL (Cell Balance Control) module provides programmable cell balancing time thresholds for each cell channel, when the timer hits any programmed time threshold, balancing for that channel is stopped (the timer continues to count and the balancing current is turned off).

### Main features

The CB\_CTRL module has the following features:

• Supports up to 18 cell channels at the same time (HWR001\_CB\_CTRL)

• Supports both automatic channel selection and manual channel selection (HWR001\_CB\_CTRL)

• Supports start (timer shall start to count and the balance current shall be on) working by register bit (HWR001\_CB\_CTRL)

• Supports outputs CB\_CH\_EN only when CB\_GO is detected (HWR003\_CB\_CTRL)

• Supports separate threshold setting for each cell channel (HWR005\_CB\_CTRL)

• Timer of balance supports be held if the JOT is H when JOT\_EN is high (HWR006\_CB\_CTRL)

•Supports being paused when any thermal sensor channel is over programmable CB\_OT threshold by register bit (HWR007\_CB\_CTRL)

•Supports being paused manually by register (HWR008\_CB\_CTRL)

•Supports being paused when channel voltage ADC measurement is ongoing (HWR009\_CB\_CTRL)

•Supports being stopped when any unmasked fault flag is set in register (HWR010\_CB\_CTRL)

The odd group and even group of battery cell channels support being switched alternately during automatic mode (HWR011\_CB\_CTRL)

•Supports programmable average cell balance current by register bit (HWR012\_CB\_CTRL)

•Provides balance current on/off indication (excluding on/off due to averaging) for each channel by register bit(HWR013\_CB\_CTRL)

•Supports configuration error detection

## Functional Details

### Block Diagram

(HWR001\_CB\_CTRL)



Fig 1CB\_CTRL Block Diagram

CB\_CTRL supports cell balancing of up to 18 channels. Only enabled channels can be balanced. The schematic diagram of CB\_CTRL is shown in Fig 1.CB\_CTRL uses shadow register internally. Except for CBFET\_ENn(n=1-18) and CB\_MANU\_PAUSE, CB will update the configuration of the register to the shadow register when CB\_GO arrives. For example, CB\_MUNAL is updated by CB\_MUNAL\_REG. Specially, CBFET\_ENn shall update with CBFET\_EN\_REGn when CB\_GO only if settings are correct. CB\_CTRL supports automatic channel selection and manual channel selection. Channel will stop balancing when reaches the threshold. When all the set channels reach the corresponding threshold, the CB will stop working.

### I/O description

Table 1 CB\_CTRL I/O description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Pin Name** | **Direction** | **Width** | **Duration** | **Description** |
| **FLT\_WAKE** | I | 1b’ | N/A | 1: to stop CB\_CTRL when FLT\_STOP\_EN =1'b1 |
| **D2A\_CELL\_ADC\_EN** | I | 1b’ | N/A | 1: to hold CB\_CTRL when ADC\_PAUSE\_EN =1'b1 |
| **JOT** | I | 1b’ | N/A | 1: to hold CB\_CTRL when JOT\_EN =1'b1 |
| **GPIO\_CBOT** | I | 1b’ | N/A | 1: to hold CB\_CTRL when GPIO\_CBOT\_EN =1'b1 |
| **CBFET\_EN\_REG** | I | 18b’ | N/A | CB\_EN Input of 18 channels |
| **CB\_GO** | I | 1b’ | N/A | To start CB\_CTRL and load CB\_Setting\_REG |
| **CB\_MANUAL\_REG** | I | 1b’ | N/A | CB mode select, 1: manual , 0:automatic |
| **JOT\_EN\_REG** | I | 1b’ | N/A | enable JOT to pause CB\_CTRL |
| **GPIO\_CBOT\_EN\_REG** | I | 1b’ | N/A | enable GPIO\_CBOT to pause CB\_CTRL |
| **ADC\_PAUSE\_EN\_REG** | I | 1b’ | N/A | enable ADC\_EN to pause CB\_CTRL |
| **CB\_MANU\_PAUSE** | I | 1b’ | N/A | pause CB\_CTRL |
| **FLT\_STOP\_EN\_REG** | I | 1b’ | N/A | enable FLT\_WAKE to stop CB\_CTRL, stop CB\_EN, and wait for another CB\_GO when FLT\_WAKE is "L" |
| **CB\_TO\_THRESH\_REG1-18** | I | 10b’ | N/A | CB threshold time about each channel |
| **CB\_UNIT\_REG1-18** | I | 1b’ | N/A | unit of CB\_TO\_THRESH\_REG |
| **CB\_PERIOD\_REG** | I | 3b’ | N/A | in automatic mode, indicate odd/even covert time, 5s-30min, 8steps refer to competitor spec |
| **CB\_TWARN\_THRESH\_REG** | I | 4b’ | N/A | after CB\_GO,CB\_CTRL output CB\_TWARN\_THRESH to analog, don’t need other operation |
| **CB\_DUTY\_REG** | I | 3b’ | N/A | duty of internal PWM, shall cover 12.5%-100%, 8steps  period is 200ms |
| **CLK\_OUT\_SC** | I | 1b’ | N/A | system clock |
| **CLK\_CB\_SC** | I | 1b’ | N/A | function clock, 256K |
| **resetb\_SR\_CLK\_OUT** | I | 1b’ | N/A | reset use for CB\_EN |
| **resetb\_SR\_CLK\_SLOW** | I | 1b’ | N/A | reset use for CLK\_CB\_SC |
| **CB\_EN** | O | 1b’ | >1 CLK\_CB\_SC | "H" when detect CB\_GO and "L" when all CH\_DONE |
| **CB\_CONF\_FLT** | O | 1b’ | 1 CLK\_CB\_SC | >2 consecutive channels turn on in CBFET\_EN |
| **clr\_CB\_GO** | O | 1b’ | >1 CLK\_CB\_SC | output to clear CB\_GO |
| **CB\_ODD\_CNT** | O | 10b’ | >=1 CLK\_CB\_SC | odd/even is same in manual mode, is different in automatic mode, counter of odd group |
| **CB\_EVEN\_CNT** | O | 10b’ | >=1 CLK\_CB\_SC | counter of even group |
| **CB\_EN\_FULL\_DUTY** | O | 18b’ | >=1 CLK\_CB\_SC | output CB\_CH\_EN with full duty |
| **CB\_TWARN\_THRESH[3:0]** | O | 4b’ | >1 CLK\_CB\_SC | after CB\_GO,CB\_CTRL output CB\_TWARN\_THRESH to analog, don’t need other operation |
| **CB\_CH\_EN** | O | 18b’ | >=1 CLK\_CB\_SC | output CB\_CH\_EN after &PWM |

### State Machine



Fig 2 State machine of detect configuration error

This state machine is mainly used to detect whether there is configuration error. That is, in manual mode, three consecutive adjacent channels are enabled. If this error occurs, CB\_CTRL will be generated CB\_CONF\_ FLT. After CB\_GO is synchronized, CB\_CTRL does not immediately enter the battery balance time, but requires fault detection first. Fault detection needs to detect a maximum of 18 channels, that is, 18 CLK\_CB\_SC.

### Mode Selection

(HWR005\_CB\_CTRL, HWR009\_CB\_CTRL)



Fig 3Waveform diagram of CB\_CTRL in automatic mode

CB\_CTRL can select the working mode by configuring CB\_MANUL\_REG, which is divided into automatic mode (CB\_MANUL=0) and manual mode (CB\_MANUL=1).For automatic mode, the enabled channels are divided into odd or even channel groups according to the channel number, and each group is cell-balanced in turn according to CB\_PERIOD, as show in Fig2.In manual mode, CB will no longer distinguish between odd and even groups, the CB\_ODD\_CNT and CB\_EVEN\_CNT counter will count together, and CB\_PERIOD will no longer work. When the counter reaches the threshold of the enabled channel, the channel will be closed, and when the counter reaches the threshold time of all channels, the CB stops working.

Table1. Grouping Details

|  |  |  |
| --- | --- | --- |
|  | Even Group | Odd Group |
| Channel Number | 1,3,5,7,9,11,13,15,17 | 2,4,6,8,10,12,14,16,18 |
| Automatic  Mode | Always Start Firstly | Always Start Secondly |
| Manual Mode | Treated as same group | |

Note: In automatic mode, even group always start counting firstly.

### Pause and Stop Control

(HWR006\_CB\_CTRL, HWR007\_CB\_CTRL, HWR008\_CB\_CTRL, HWR009\_CB\_CTRL, HWR010\_CB\_CTRL)

CB\_CTRL supports pausing or stopping during cell balancing. When suspending, turn off the corresponding suspend signal, CB\_CTRL can resume work, but can only be restarted by CB\_GO after stopping.

Table2. Conditions for pause and stop of CB

|  |  |  |
| --- | --- | --- |
|  | Pause | Stop |
| 1 | CB\_MUNU\_PAUSE\_REG | FLT\_WAKE &FLT\_STOP\_EN\_REG |
| 2 | D2A\_CELL\_ADC\_EN & ADC\_PAUSE\_EN\_REG |
| 3 | JOT & JOT\_EN\_REG |
| 4 | GPIO\_CBOT &GPIO\_CBOT\_EN\_REG |

### Internal Pulse Width Modulation

(HWR012\_CB\_CTRL, HWR013\_CB\_CTRL)

CB supports pulse width modulation (PWM) of CB\_EN\_FULL\_DUTY. The period after PWM is fixed at 200ms, and there are 8 kinds of adjustable duty cycles, which are controlled by CB\_DUTY\_REG.



Fig 3 Schematic diagram of a PWM with a duty cycle of 1/2

### Fault Detection

When CB\_MUAL is configured to 1(manual mode), a configuration error judgment will be carried out. If there is a configuration error, CB\_CTRL will immediately end and generate CB\_CONF\_FLT. When CB\_CONF\_FLT\_MSK is 0, CB\_CONF\_FLT will be written to the FAULT register.